

# Modified Cascaded Five Level Multilevel Inverter Using Hybrid Pulse Width Modulation

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**Abstract**— Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. Such inverters synthesize a desired output voltage from several levels of dc voltages as inputs. Our aim in this project is to analyze the performance of cascaded five level inverter using hybrid pulse width modulation technique. It has been found that this technique reduces the switching losses and total harmonic distortion. In the conventional cascaded H-bridge multilevel inverter eight power switches have been used is reduced to six power switches by employing this topology and it can be employed for high voltage and high power applications. Due to these advantages, cascaded H-bridge inverter has been widely applied to such applications as HVDC, SVC, stabilizers, and high power motor drives. The performance can be analyzed by the MATLAB/Simulink.

**Keywords**—Multilevel inverter, Cascaded H-Bridge multilevel inverter, Hybrid pulse width modulation, Total harmonic distortion.

## I. INTRODUCTION

A multilevel inverter is a power electronic converter that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic compatibility, and lower switching losses.

High magnitude of sinusoidal voltage with extremely low distortion at fundamental frequency can be produced at output with the help of multilevel inverter by connecting sufficient number of dc levels at input side. Multilevel inverter can increase the power by (n-1) times than that of two level inverter through series and parallel connection of power semiconductor switches.

A cascaded multilevel inverter consists of a series of H-bridge inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate DC sources, which may be obtained from batteries,

fuel cells, or solar cells. A particular advantage of this topology is that the modulation, control and protection requirements of each bridge are modular.

## II. CASCADED FIVE LEVEL MULTILEVEL INVERTER

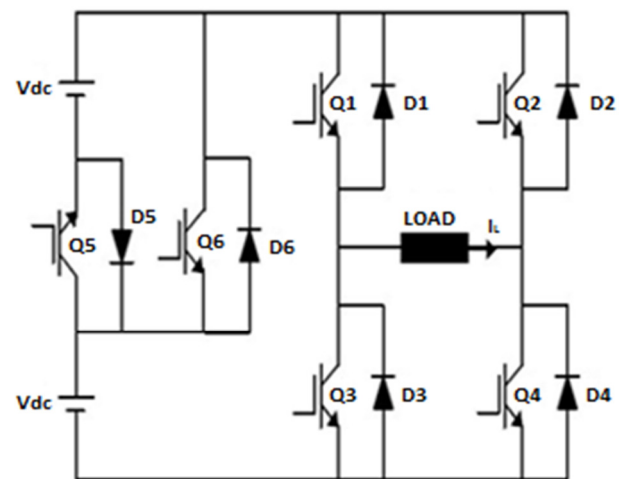


Fig.1. 1-Φ Modified cascaded five level inverter

The 1- $\Phi$  cascaded five level inverter topology has been proposed to reduce the number of power switches when compared to the conventional cascaded H-bridge multilevel inverter. A modified 1- $\Phi$  cascaded five level inverter topology is shown in Fig. 1. The circuit consists of four main switches in H-bridge configuration Q1-Q4, and two auxiliary switches Q5 and Q6. The number of dc sources (*two*) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter so that the output voltage of the cascaded multilevel inverter is  $V(t) = V_1(t) + V_2(t)$ . Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig.2

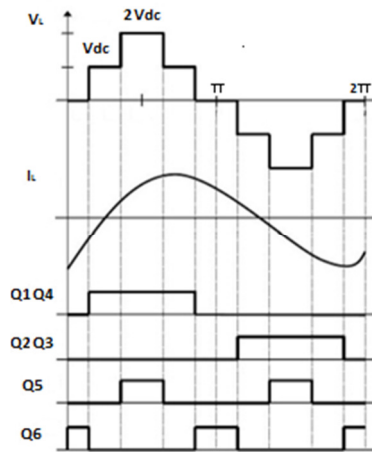


Fig.2. Waveforms of the proposed five level inverter topology

### III. OPERATION OF PROPOSED 1- $\Phi$ FIVE LEVEL INVERTER

The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes are powering mode, freewheeling mode and regenerating mode.

#### 1. Powering Mode

This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is  $V_{dc}$ , the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is  $2V_{dc}$ , current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

#### 2. Free-Wheeling Mode

Free-wheeling modes exist when one of the main switches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.

#### 3. Regenerating Mode

In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source.

Table 1  
Switching Strategy

Voltage	Q1	Q2	Q3	Q4	Q5	Q6
$-2V_{dc}$	0	1	1	0	1	0
$-V_{dc}$	0	1	1	0	0	0
0	1	0	0	1	0	1
0	0	1	1	0	0	1
$V_{dc}$	1	0	0	1	1	0
$2V_{dc}$	1	0	0	1	1	0

### IV. HYBRID PWM TECHNIQUE

In PWM technique pulses of unequal widths are generated. The pulse is generated by comparing a sinusoidal wave (modulating signal) of frequency 50HZ against a triangular wave (carrier signal). Each comparison gives one if the modulating signal is greater than the triangular carrier else zero. The number of pulses per cycle is decided by the ratio of the triangular carrier frequency to that of the modulating sinusoidal frequency. The main inverter refers to H2 bridge and the auxiliary inverter refers to H1 bridge. Since the low switching losses during PWM operation is required, the main inverter will operate only at square wave mode and auxiliary inverter will operate at PWM mode.

It is developed to reduce number of power switches & switching losses. Technique uses combination of square wave mode and SPWM mode. In H-bridge multilevel inverter, main inverter operates on square wave mode and auxiliary inverter operates on SPWM mode.

## V. SECOND ORDER LOW PASS FILTER

Second Order Filters which are also referred to as VCVS filters, because the op-amp is used as a Voltage Controlled Voltage Source amplifier, are another important type of active filter design because along with the active first order RC filters, higher order filter circuits can be designed using them. Second order low pass filters are easy to design and are used extensively in many applications. Second order low pass filter circuit has two RC networks, which give the filter its frequency response properties.

## VI. SIMULATION RESULTS

In this paper, the simulation model is developed with MATLAB/simulink. The simulation results of proposed five level inverter and the corresponding FFT analysis are shown in fig.3.

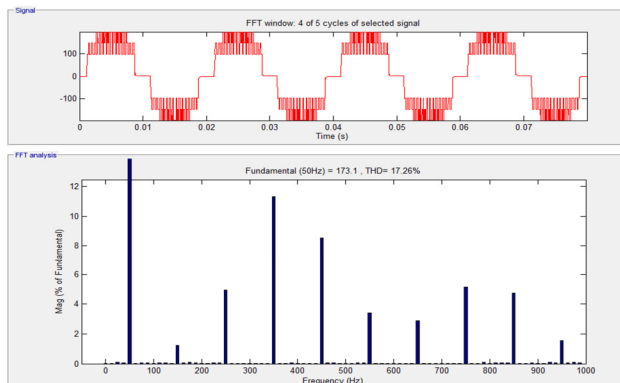


Fig.3 Waveforms & FFT analysis of proposed 5 level inverter

Also the simulation results and FFT analysis of proposed inverter connected with 2<sup>nd</sup> order LPF are shown in fig.4 including transient period & fig.5 only steady state period.

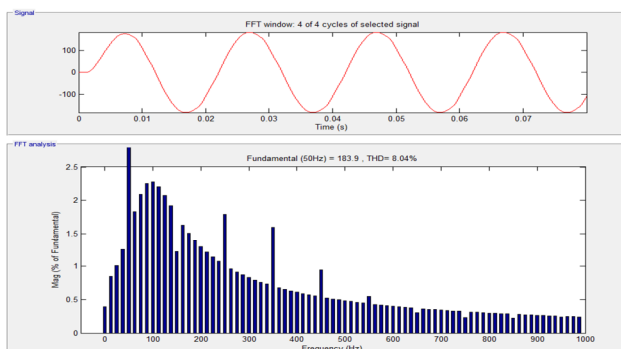


Fig. 4 Waveforms & FFT analysis of proposed 5 level inverter with LPF considering transient starting period

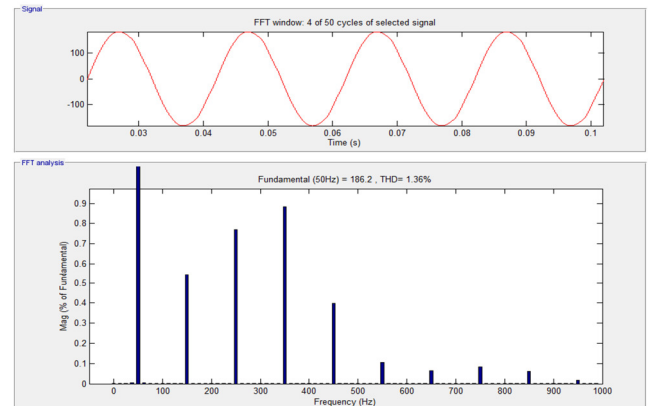


Fig. 5 Waveforms & FFT analysis of proposed 5 level inverter with LPF considering steady state period

## VII. CONCLUSION

In the Present Work, performance of cascaded five level inverter using hybrid pulse width modulation technique has been analyzed. The topology used in this technique reduces the number of power switches and switching losses. In the conventional cascaded H-bridge multilevel inverter eight power switches have been used is reduced to six power switches by employing this topology and it can be employed for high voltage and high power applications. The performance has been analyzed by the MATLAB/Simulink. The simulation output shows favorable result with a minimum total harmonic distortion of 17.21%. After connecting 2<sup>nd</sup> order LPF to the proposed 5 level inverter, the output waveform becomes pure sinusoidal with better THD results as 8.04% if starting transient period is considered. In steady state, lowest THD results are observed up to 1.36%.

## REFERENCES

- [1] "POWER ELECTRONICS HANDBOOK", Third Edition by Muhammed H. Rashid
- [2] S. Sivagamasundari, Dr. P. Melba Mary (IJETA), "Analysis of cascaded 5 level multilevel inverter using hybrid PWM" Volume 3, Issue 4, April 2013
- [3] John N. Chiasson, Leon M. Tolbert, Keith J. McKenzie, Zhong Du, "A Complete solution to the harmonic elimination problem", IEEE transactions on power electronics, Vol. 19, No.2, pp. 491-498, March 2004.
- [4] C. Kiruthika, T. Ambika, Dr. R. Seyezhai, "Simulation of cascaded multilevel inverter using Hybrid PWM technique", International Journal of Systems, Algorithms & Applications, Volume 1, Issue 1, December 2011

- [5] Indrajit Sarkar and B. G. Fernandes, "Modified Hybrid Multi-Carrier PWM Technique for Cascaded H-Bridge Multilevel Inverter" Department of Electrical Engineering, IIT Bombay, Volume 1, Issue 1, December 2011.
- [6] Zhou Jinghua, Li Zhengxi, "Research on Hybrid Modulation Strategies Based on General Hybrid Topology of Multilevel Inverter" International Symposium on Power Electronics, Electrical Drives, Automation and Motion, North China University of Technology, Beijing, (China), 2008.

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