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Design and Analysis of 3 Stage OP AMP for VLSI Applications

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Abstract **-** Relentless scaling to minimum dimensions for achieving higher packing density, reduced power dissipation and aggrandized integrated circuit speed, has made CMOS a prevailing technology for very large scale integration (VLSI) applications in the last few decades. CMOS operational amplifier (Op Amp) as a building block in analogue integrated circuits and mixed signal system has compelled researchers to execute efficient designing model and its analysis. This study was aimed to accomplish the design, simulation and inquisitive behavioral analysis of a Three-Stage OP-AMP at 100 nm technology node using 1 volt as power supply (Vdd). Transfer function, input resistance, output resistance, average power, slew-rate, phase margin, DC gain and many other parameters were duly taken into consideration during simulation processes. High DC gain (69.69 dB), high bandwidth (52.619 KHz), low output resistance (25.0718 ohm.) and low power dissipation were achieved successfully by applying the designed model proposed in the present study which satisfy the requirement of highly efficient Op Amp. This CMOS-dependent-three-stage OP AMP architectonic with various promising specifications is suitable for applying in different amplifier architectures and other related designs in nano level CMOS technology.

Keywords—CMOS, Three-stage op-amp, Low voltage, Transistors, DC gain.

I. INTRODUCTION

Exponential improvement in the performance of integrated circuits has been on rise for last few decades. Upgraded integrated circuit speed, reduced power dissipation, greater packing density have been the ideal necessities of electronic industries globally. Such worldwide global requirements have fostered the researchers to continual relentless scaling of CMOS technological processes to much smaller dimension in particular at the level of nano scale in achieving the need of very large scale integration (VLSI) industries [1,2]. CMOS has become a prevailing technology for very large scale integration (VLSI) applications in the recent years [3]. CMOS operational amplifier (Op-Amp) as a building block in analogue integrated circuits and mixed signal system. However, it is also necessary to overcome various CMOS technological challenges for sustainable scaling of the processes [4,5]. Lower headroom for analogue design appears as a consequence of inconformity of transistor's threshold voltage with V_{DD} during the process of CMOS device scaling. With the application of transistor intrinsic gain architecture, CMOS-operational amplifier (op amp) DC gain may be predicted [6]. Operational amplifier is considered to be a bottleneck of any analogue circuit. Ideally they perform the function of a voltage controlled current source along with an infinite level of voltage gain. They are applied in vast range of circuits encompassing data-converters, filters, voltage references and power management circuits. OP-AMPs with greater complexity are used to know essential functions that ranges from DC bias production to high-speed amplification or filtering process. OP-AMPs designing constantly posing challenges as the supply voltage and channel lengths of transistors scale down with every new generation of CMOS technological processes [7]. In order to achieve the gain necessities of an OP-AMPs at nano level CMOS technology with low supply voltage (1 volt), 3 or even more stage OP-AMPs topologies have recently become remarkably significant. And thus, In the present study accomplishment of the design, simulation and inquisitive behavioral analysis of a Three-Stage OP-AMP at 100 nm technology node using 1 volt as power supply (Vdd) was undertaken.

II. RELATED WORK

Design of multistage OP-AMP is a challenging work because of high impedance nodes which leads to stability related issues and to stabilize the OP-AMP various compensation technological processes have been proposed [8]. Apart from these challenges the variation in process has become prominent that leads to the remarkable offsets in OP-AMP owing to device mismatch [9,10].

A three-stage op-amp compensation: A reversed nested compensation topology is used so that the output is not loaded by both of the compensation capacitors that leads to a larger unity gain frequency [11,12]. A stack of maximum three transistors is used to realize the low-V_{DD} gain stages. In this topology an NMOS diff-amp is cascaded with a PMOS diff-amp which is followed by a class output buffer [13]. The PMOS diff-pair in second stage employs wider devices to enhance the input common-mode range of the second stage. A diff-amp is employed in the second stage to ensure that the third stage is properly biased by

symmetry [14]. The compensation capacitor is used to feedback the compensation current from the output of the second stage to the output of the first stage through a common gate current buffer. Similarly, capacitor is used to feedback current.

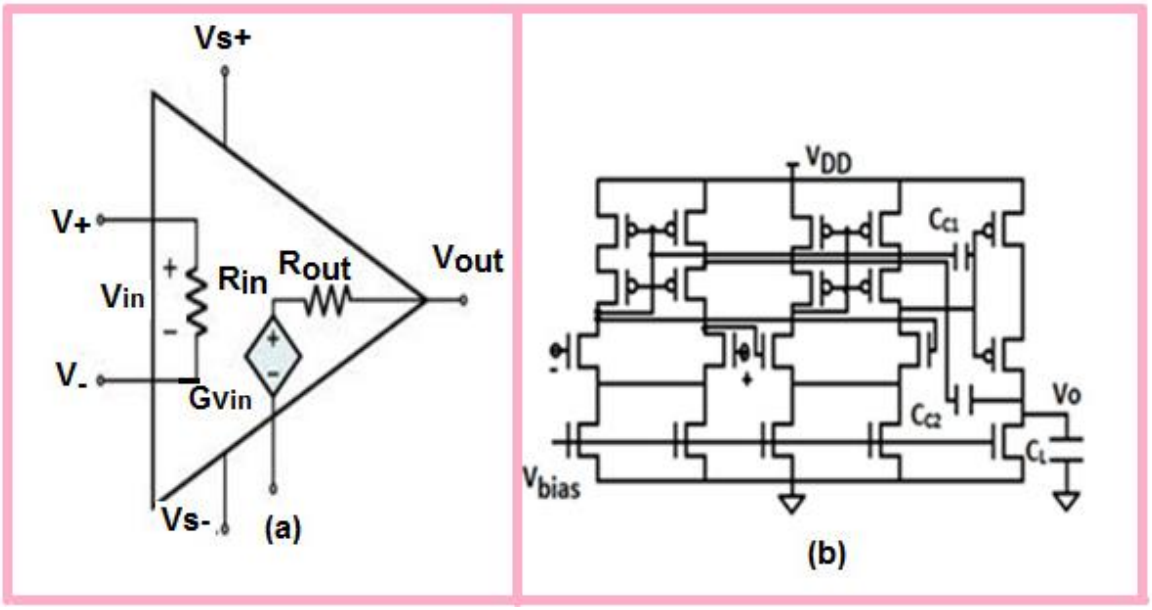

Figure 1. (a) Equivalent circuit of an Operational Amplifier (b) Proposed three-stage op-amp

If a resister load is connected to the output of the common-source stage, the overall op-amp gain remains relatively high owing to the cascaded gain of the diff-amps. The primary concern with this topology (an Op-Amp with greater than two stages) as per previous allusion is compensation and the way current through Ccl feeds back to node 1 through the diode-connected load of the input diff-amp [15]. This is very important to ensure that the signal through Cc1 adds with the signal fed back directly to node 1 through Cc2.

III. METHODOLOGY

Three-Stage OP-AMP designing, simulation and inquisitive analysis of its behaviour were carried out at 100 nm technology node using 1 volt as power supply (Vdd). Applying high frequency, the design of three-stage op-amp may be regarded as a non-linear optimization of a number of variables. Iterative design procedure was opted in order to meet required set of desirable specifications. Transfer function, input resistance, output resistance, average power, slew-rate, phase margin, DC gain in dB and many other parameters were duly taken into consideration during simulation processes. Initialization of process with parameters such as capacitive load (C_L) and slew rate (SR) while DC gain was distributed across the stages. Setting up of Vgs, f_T and $g_m r_o$ was carried out by selecting overdrive process. A specific value for gm1 and gm2 were selected for the desired phase margin (PM) which has been depicted in Fig-2. Slew-rate (SR) was improved by enhancing the bias current in the first stage.

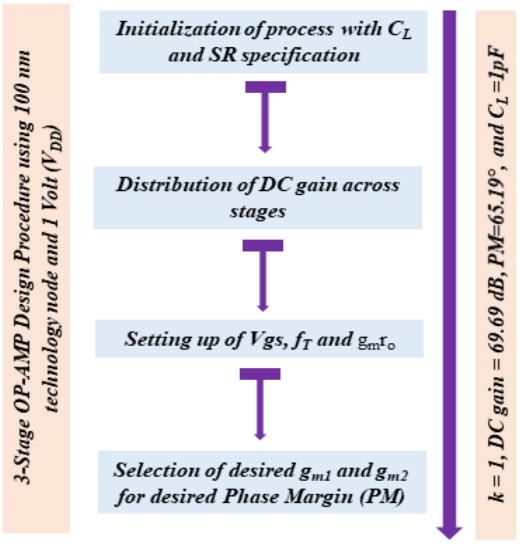

Figure 2. Workflow of design procedure

IV. RESULTS AND DISCUSSION

Performance enhancement of an integrated circuit in exponential manner has been constantly growing. Recently focus of researchers have been on enhancing integrated circuit speed, reducing power dissipation, increasing packing density by scaling CMOS technology to nano level dimensions [1-3]. CMOS has got the place a prevailing technology for very large scale integration (VLSI) applications electronic industries. CMOS operational amplifier (Op-Amp) as a building block in analogue integrated circuits and mixed signal system has been used all sections of electronics [16]. Designing, simulation and inquisitive analysis of its behaviour of the

Three-Stage OP-AMP were carried out at 100 nm technology node using CMOS process. Comparative analysis of op amps including Three-Stage OP-AMP and the level of distortion with varying frequencies have been reported by Hernes et al., 2005 [17] suggesting that the three-stage op amp has much lower distortion at reduced frequencies. Applying high frequency, the design of three-stage op-amp may be regarded as a non-linear optimization of a number of variables [17]. Power supply voltage was set to 1V, k = 1, C_L=1pF were set as design specifications. Modelling and simulation of Three-Stage op-amps at 1V using AC analyses have been shown in Fig-3 and Fig-5 while that using transient analysis has been depicted in Fig-4. Width and length for PMOS and NMOS were calculated that has been tabulated in Table 2. The performance of the designed Three-Stage OP-AMP in terms of achieved values of various significant parameters has been demonstrated in Table 1. High DC gain (6.9695 x 10^1 dB) achieved successfully by applying the designed model proposed in the present study which satisfy the requirement of highly efficient Op-Amp. And this finding of high DC gain is comparatively than that in similar study conducted by Solanki *et al.* [18] This level of high DC gain achieved by current model also corroborates with the similar findings of Bult *et al.* [19] Achieving high gain is the primary focal point in electronic circuit design which may also been accomplished by incorporating fundamentals of cascode in the CNTFET-based OTAs for a considerable enhancement in gain (12.5%) and output resistance (13.07%) [20,21]. High bandwidth (5.2619 x 10^4 GH_z), output resistance (25.0718 ohm.) and low power dissipation have been achieved too using the present design architecture which fulfils the requirement of higher efficiency of Op-Amp which is comparable with the findings of a similar investigation by Vadodaria *et al.* [22] Respective widths of PMOS transistors were recorded to be twice that of NMOS-transistors whereas the PMOS transistors' respective length were calculated to be half that of the NMOS transistors. This CMOS-dependent-three-stage OP-AMP architectonic with various promising specifications recorded in this study is suitable for applying in different amplifier architectures and other related designs in nano-level CMOS technologies which may also be used in design of an operational trans-conductance amplifier (OTA) [23]. CMOS scaling to much lower dimensions especially in low power and high speed devices needs to be continuously executed for further enhancement of electronic devices.

$$DC\ Gain = g_{mn1}(r_{on1} \parallel r_{op1}) \cdot g_{mn2}(r_{on2} \parallel r_{op2}) \cdot g_{mp3}(r_{on3} \parallel r_{op3}) \quad (1)$$

The unity-gain frequency is given by

$$f_{un} = g_{mn} / 2\pi\,(C_{c2} + C_{c1}/A_3) \quad (2)$$

Where $g_{mn1}(r_{on1} \parallel r_{op1})$, $g_{mn2}(r_{on2} \parallel r_{op2})$ and $g_{mp3}(r_{on3} \parallel r_{op3})$ are the gain of 1st differential amplifier, 2nd differential amplifier and common source respectively [24].

Modelling and simulation of three-Stage op-amps at 1V using AC analysis.

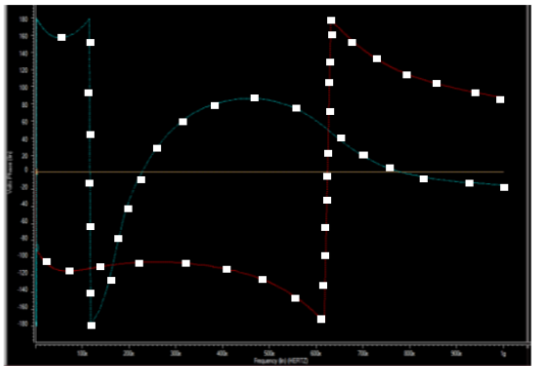

Figure 3. Input and Output phase voltage Waveform

Modelling and simulation of three-stage op-amps at 1V using transient analysis

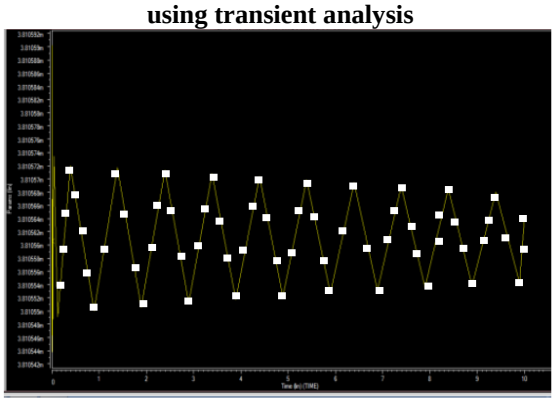

Figure 4. Average Power waveform

Modelling and simulation of a three-Stage op-amps at 1V using AC analysis.

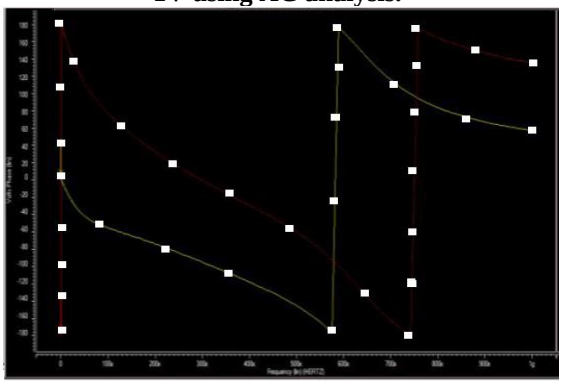

Figure 5. voltage magnitude biasing

Table 1. Performance Measuring Parameters of the proposed Three-stage op-amp

S.N.	Parameters	Value
1	DC Gain	69.69dB
2	Bandwidth	52.619 KH_z
3	Output resistance	25.0718 ohm
4	Trans-conductance	1.0004 mS
5	Input resistance	1.4045k ohm
6	Phase margin	65.19^0
7	Slew-rate	59.83V/µs
8	Average power	96.155 µw

Table 2. Selected width and length for the transistors used

Width of P-MOS Transistors		Width of N-MOS Transistors		Length of P-MOS Transistors		Length of N-MOS Transistors	
M3T1	5000nm	M11	2500nm	M3T1	50nm	M11	100nm
M3B1	5000nm	M21	2500nm	M3B1	50nm	M21	100nm
M4T1	5000nm	M6L1	2500nm	M4T1	50nm	M6L1	100nm
M4B1	5000nm	M6R1	2500nm	M4B1	50nm	M6R1	100nm
M3T2	5000nm	M12	2500nm	M3T2	50nm	M12	100nm
M3B2	5000nm	M22	2500nm	M3B2	50nm	M22	100nm
M4T2	5000nm	M6L2	2500nm	M4T2	50nm	M6L2	100nm
M4B2	5000nm	M6R2	2500nm	M4B2	50nm	M6R2	100nm
M7T	5000nm	M8	2500nm	M7T	50nm	M8	100nm
M7B	5000nm			M7B	50nm		

V. CONCLUSION AND FUTURE SCOPE

CMOS operational amplifier (Op-Amp) as a building block in analogue integrated circuits and mixed signal system has gain the attentions of research across the globe in the recent years. Continuous CMOS scaling to minimum dimensions particularly at nano-scale level has greatly improved the transistor speed at minimum feature size. In the current investigation the systematic design, simulation and analysis of behaviour of three stage Op-Amp for high frequency applications was accomplished. High DC gain, high bandwidth, low output resistance and low power dissipation have been achieved by applying the designed model proposed in the study that fulfils the necessities of highly efficient Op-Amp. This CMOS-dependent-three-stage OP-AMP architectonic with various promising specifications is suitable for applying in different amplifier architectures and other related designs in nano-level CMOS technologies. Further nano-scale designing and CMOS scaling especially in low power and high speed devices in the modern day electronics may be studied for enhancing the efficiency of future generation of electronic devices.

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