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Various Design Architectural level Power Reduction Techniques for Viterbi Decoder: A Review

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Abstract— The Viterbi algorithm is commonly applied in a number of sensitive usage models including decoding convolutional codes used in communications such as satellite communication, cellular relay, and wireless local area networks. The Viterbi algorithm process is similar to finding the most-likely sequence of states, resulting in sequence of observed events and, thus, boasts of high efficiency as it consists of finite number of possible states. Viterbi decoder is very important part at the receiver side in order to decode the convolutional codes. This paper briefly reviews the power reduction techniques along with their comparative analysis for designing Veterbi decoder at the receiver side of convolutional codes.

Keywords— Viterbi Decoder, BMU, PMU, SMU, ACS

I. INTRODUCTION

Now a days in digital communication systems, convolutional codes are one of the key part in channel coding techniques. In order to handle the continuous data stream and blocks of data convolution coding plays vital role and provides many more advantages. While decoding the convolution codes, Viterbi algorithm [1] is widely used due to its high performance. It is one of the important part in various communication standards like satellite, Wireless Local Area Network (WLAN), and so on.

Viterbi decoder is the most suitable hardware platform for implementing the Viterbi algorithm. Since communication is the fast growing field now a days, creates Fast developments in the field of communication in the recent years have created a expanding demand for high speed and low power Viterbi decoders with better battery life. Figure 1.1 shows the block diagram of channel encoder and decoder which includes convolutional encoder and Viterbi decoder of Digital communication system.

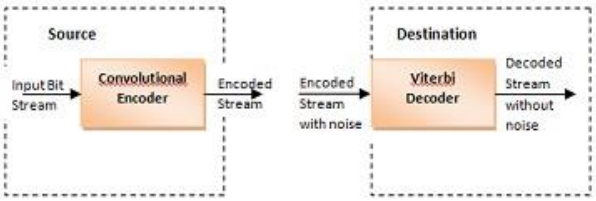

Fig 1.1 Block diagram of channel encoder and decoder for Digital communication system

As shown in the above figure 1.1 Viterbi decoder is one of the key components in digital communications as well as storage devices. Previously researchers had worked on its VLSI implementation, still every new design has its own technological exploration. In order to acquire the basic knowledge of veterbi decoder, next part will focus on viterbi decoder and its parts.

1.1 Viterbi Decoder

The block diagram of the Viterbi decoder is shown in Figure 3.1. It is composed of three functional units:
(1) Branch Metric Unit (BMU).
(2) PathMetric Unit (PMU) or Add Compare Select Unit (ACSU).
(3) Survivor Memory Unit (SMU).

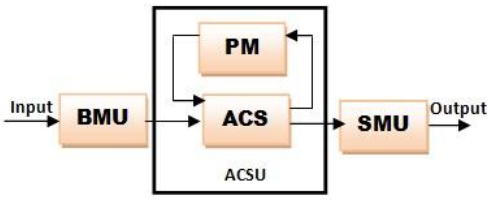

Figure 1.2 Block Diagram of Viterbi Decoder

Function of BMU:

BMU, the first unit, consists of XOR gate and counter. The branchmetric (BM) computation block compares the received code symbol with the expected cod symbol and counts the number of differing bits. The BMU for one state is given in Figure 1.3**.**

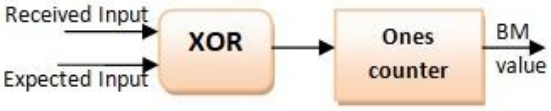

Figure 1.3 BMU for one state

Working of ACS Unit:

The second unit in the Viterbi decoding is ACSU which is the heart of the process and dictates the performance of the

decoder. The ACS operation for each new state in the trellis performs the addition, comparison, and selection of the smallest path metric (PM). Figure 3.3 shows the block diagram of the ACS module

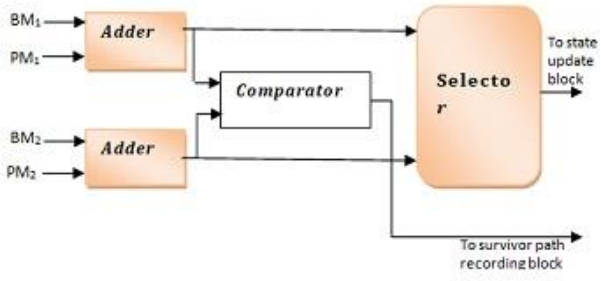

Figure 1.4 Block diagram of ACS Module

Function of SMU:

To find the survivor path entering each state of the decoder, the BM of a given transition is added to its corresponding PM. This sum (BM + PM) is compared to all the other sums corresponding to all the other transitions entering that state. The transition that has the minimum sum is chosen to be the survivor path. The third step in the Viterbi decoding is SMU.

Low power dissipation and low weight regardless of the significant progress in the last decade, the problem of power dissipation in the Viterbi decoders still remains challenging and requires further technical solutions. Thus, a flexible, low power, and high speed Viterbi decoder design is a key challenge for future portable and communication devices. Next part of this paper reviews various power reduction techniques given by various researchers.

Viterbi decoder is very important part at the receiver side in order to decode the convolutional codes. There is enormous research is going on designing viterbi decoder and researchers are getting success in same but still designing of viterbi decoder which consumes less power is the area of interest. In the next section some literature which is associated to the power reduction techniques is reviewed along with a table viewing combine analysis of these methods.

In this paper next session includes brief review of literature of power reduction techniques of viterbi decoder along with proposed methodology of work and expected results of proposed work.

II. LITERATURE SURVEY

Burcu Ozbay et. al 2018 [2] proposes a method in which a power- and area-efficient Viterbi decoder architecture that also reduces the computational complexity is proposed. Initially, in this technique a hard-decision Viterbi decoder system architecture design for Very Large Scale Integration (VLSI) realization was fulfilled without any further improvement to compare the performance of fundamental and improved designs with respect to power consumption. The architectural design is described using the Verilog hardware description language for comparing the related tests and performance of FPGA platform. Convolutional encoder with constraint length 3 and code rate 1/2 and the decoder decoding this code has been designed and implemented and decoder has been developed as power efficient. The key consideration of this work is to decrease the power dissipation and Power consumption on hardware has been reduced to half.

Waqar Ahmad et. al 2018 [3] propose a method for enhancement in DLX and Pico- Java II processor ISA for efficient implementation of Viterbi decoding algorithm. This technique creates a custom trellis expansion instruction (Texpand) in CPUSIM simulator on RISC based architecture and MIC-1 simulator on stack based architecture. The execution time is stupendously improved to approximately three times, when Texpand instruction is designed for RISC architecture and approximately three times for stack based architecture. In addition, this method enhances the ISA of NIOS II soft processor for the efficient implementation of Viterbi algorithm. The comparison with and without the custom instruction shows substantial improvement in the results. The performance of the NIOS II processor with the custom instruction is improved to two times to the assembly language program without the custom instruction.

However, an FPGA based implementation of these processors may also improve the execution performance for computationally complex algorithms as the clock frequency can be change and also execute the custom instruction in parallel to other independent instructions.

S.Nanthini Devi et. al 2017[4] proposes a method for wireless communication, by taking into the consideration of demand for high speed, low power and low cost Viterbi decoding. In this work Convolutional coding with Viterbi decoding is used which is very powerful method for forward error correction and detection method. From this research it can be conclude that if trace back is started after going deeper into trellis diagram then more accurate data can be achieved but it results in complex hardware design and latency in the received signal. Viterbi algorithm of any rate can be designed using same basic principles and its techniques.

Dinesh Kumar et. al 2017 [5] designed a high speed feed forward viterbi decoder using hybrid track back and register exchange architecture and embedded BRAM of target FPGA. this viterbi decoder has been designed with Matlab, simulated with Xilinx ISE 8.1i Tool, synthesized with Xilinx Synthesis Tool (XST), and implemented on Xilinx Virtex4 based xc4vlx15 FPGA device. The results show that the proposed design can operate at an estimated frequency of 107.7 MHz by consuming considerably less resources on target device to provide cost effective solution for wireless applications. The results of proposed design can work at an estimated frequency of 86.6 MHz by using considerable less resources of target FPGA to provide high performance cost effective solution for wireless communication applications.

Mohd Azlan Abu et al 2016 [6] designed a Viterbi decoder for low power consumption space time trellis code without adder architecture using RTL model. This research aims to describe the real-time design and implementation of a Space Time Trellis Code decoder using Altera Complex Programmable Logic Devices (CPLD). The code uses a generator matrix designed for four-state space time trellis code (STTC) that uses quadrature phase shift keying (QPSK) modulation scheme. This research gives comparative analysis between previous CPLD devices for the STTC Viterbi decoder design. The result shows that this proposed design can work with a 96 per cent improvement in power consumption for a targeted MAX V CPLD board compared to the experiences reported in the previous methods. The decoding process has been carried out using maximum likelihood sequences estimation through the Viterbi algorithm. This work showed that the STTC decoder can successfully decipher the encoded symbols from the STTC encoder and can fully recover the original data. The data rate of the decoder is 50 Mbps.

T. Kalavathi Devi et. al 2015 [7] designed an asynchronous low power and high Performance VLSI architecture for Viterbi decoder implemented with quasi delay insensitive templates. Designed decoder meets the demand of high speed and low power. At present, the design of a competent system in Very Large Scale Integration (VLSI) technology requires these VLSI parameters to be finely defined. The proposed asynchronous method focuses on reducing the power consumption of Viterbi decoder for various constraint lengths using asynchronous modules. The result of this work shows that the design flow using asynchronous can yield good performance with 25.21% decrease in power consumption compared to the synchronous method.

T. Kalavathi Devi et. al 2012 [8] proposed the low power VLSI architecture asynchronous technique [16, 17] is applied for only BMU and ACS unit. The analysis of power dissipation shows variation in the integrated design of Viterbi decoder. The entire design does not involve the sequence of the state transition graph of PCHB and WCHB buffers. Hence further development of thework concentrating on the complete asynchronous design with buffers and control signals is carried out.The decoder is designed only for the constraint length K = 3 while encoder is designed for K = 3 to 7 and the results of the encoder are verified for the decoder architecture K = 3. It is found that the number of transistor counts ismore in asynchronous design for K = 3 as the design was simulated on Tanner 7.0 completely in transistors, which leads to the increase in area.

K.Cholan 2011 [9] works on design and implementation of low power high speed Viterbi decoder The algorithm tries to find a path of the trellis diagram, where the sequence of output symbols approximately matches the received sequence. To accomplish this task, it calculates for each path the path metric, which measures the distance to the received symbols sequence. A new method of viterbi decoder is presented in this research. The design is based on re- configurable FPGA technology, by adopting parallel/pipeline features of the hardware resources. The exiting algorithm is redesigned using HDL language, simulation, synthesis and implementation (translation, mapping place & routing) done with FPGA based EDA tools. The overall system performance improved in terms of area and speed.

III. PROPOSED METHHODOLOGY

The main problem faced while designing viterbi decoder VD is power consumption. In previous section of this paper various methods are discussed for designing of VD which consumes less power. Proposed method mainly concentrate on designing of VD which consumes less power while in order to achieve the objective of reducing the power consumption of viterbi decoder without degrading its performance power reduction techniques are used**.** The top level architecture of the VD is shown below.

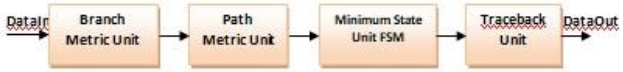

Figure 3.1 The top level architecture of the Viterbi decoder

There are three main stages while designing power efficient VD which are, Branch Metric Unit, Path Metric Unit and Traceback Unit . All the three stages come together to decode the received message that is transmitted over a digital channel after appropriate convolution encoding to introduce appropriate redundancy in the transmitted message Low power design strategy of proposed method is as follows:

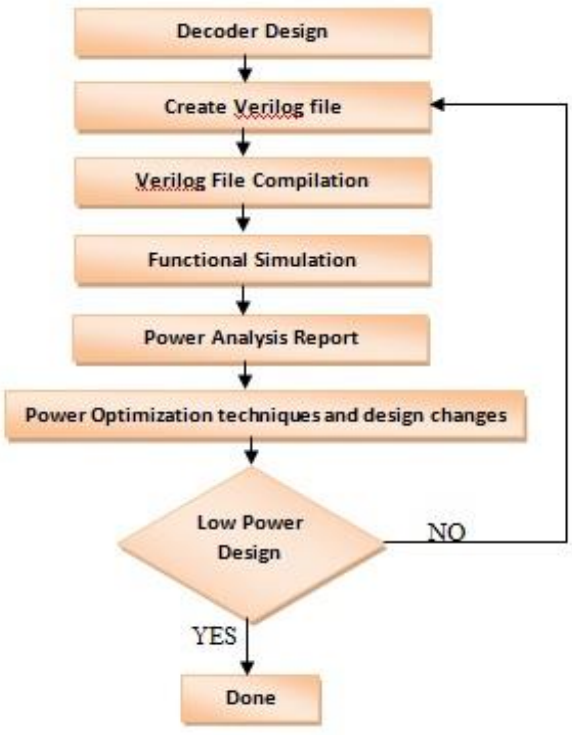

Figure 3.2 Low power design strategy of proposed method

If Pipelining, Clock gating, Parallelism methods will be used in designing various blocks of Viterbi decoder it will provides better results regarding power reduction of VD as, Clock gating reduces dynamic power dissipation by reducing unnecessary switching activity in the digital circuit, in parallelism VDD technique, where non critical paths can be powered by lower supply voltage to reduce overall power and data path pipelining reduces critical path lengths, and therefore can be used to reduce dynamic power dissipation.

IV. EXPECTED RESULTS

Out of the three methods mentioned above conventional trace back approach takes the largest area and proposed low power design takes least area. The area of the proposed pipelined low power design wills considerably less than that of the conventional approach. Proposed architecture will provides low power dissipation as the size of the decoder is very small.

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V. CONCLUSION

A range of applications like LANs, ultra wide band systems, and digital mobile communications in which Viterbi decoder is in use, are complex in their implementation and they dissipate large power. Numerous methods are existing for designing the Viterbi decoder, but key consideration while designing Viterbi decoder is less power consumption. In this paper various power reduction techniques for viterbi decoder is reviewed along with the comparative analysis of these methods is given. If Pipelining, Clock gating, Parallelism methods will be used in designing various blocks of Viterbi decoder it will provides better results regarding power reduction of Viterbi decoder.

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Table 2.1 Comparison of various power reduction techniques of Viterbi Decoder

Year	Author	Method	Description
2018	Burcu Ozbay et. al	A power efficient VD is to reduce the computational and hardware complexity	Decrease the power dissipation in accordance with this purpose presented a T-algorithm for power efficient management in VD.
2018	Waqar Ahmad et. al	Custom Instruction Approach	Report an enhancement in DLX and Pico- Java II processor ISA for efficient implementation of Viterbi decoding algorithm and creates a custom trellis expansion instruction (Texpand) in CPUSIM simulator on RISC basedarchitecture and MIC-1 simulator on stack based architecture
2017	S.Nanthini Devi et. al	Convolutional Coding with Viterbi Decoding using FSM	If trace back is started after going deeper into trellis diagram then more accurate data can be achieved but it results in complex hardware design and latency in the received signal. Viterbi algorithm of any rate can be designed using same basic principles and its techniques.
2017	Dinesh Kumar et. al	Matlab, simulated with Xilinx ISE 8.1i Tool, synthesized with Xilinx Synthesis Tool (XST), and implemented on Xilinx Virtex4 based xc4vlx15 FPGA device	A high speed Viterbi decoder has been proposed. The embedded BRAM and LUTs of target FPGA have been efficiently utilized to enhance the speed of the developed decoder.
2016	Mohd Azlan Abu et al	Trellis code without adder architecture using RTL model	The results showed that the STTC decoder can successfully decipher the encoded symbols from the STTC encoder and can fully recover the original data. The data rate of the decoder is 50 Mbps.
2015	T. Kalavathi Devi et. al	Viterbi decoder implemented with quasi delay insensitive templates	Design flow using asynchronous can yield good performance with 25.21% decrease in power consumption compared to the synchronous method.
2012	T. Kalavathi Devi et. al	The low power VLSI architecture asynchronous technique is applied for only BMU and ACS units.	The number of transistor counts is more in asynchronous design for K = 3 as the design was simulated on Tanner 7.0 completely in transistors, which leads to the increase in area.
2011	K.Cholan	Re-configurable FPGA technology	The exiting algorithm is redesigned using HDL language, simulation, synthesis and implementation (translation, mapping place & routing) done with FPGA based EDA tools. The overall system performance improved in terms of area and speed.

Authors Profile

Miss J. J. Zunzunwala completed her bachelor of Engineering from SGBAU Amravati university and Master of technology from RTM university, Nagpur. She had more than 7 years of teaching experience in P. R. Pote college of engineering and Management Amravati as a Assistant professor in ExTC. Currently she is persuing her Doctors from SGBAU Amravati university. Her research work focuses on Power Reduction Techniques for Viterbi Decoder.

Dr Atul S Joshi completed his PhD in year 2014 from Sant Gadge Baba Amravati university, Amravati. He is currently working as Professor & Dean PhD cell in Sipna College of Engineering & Technology, Amravati. He has 22 Years of teaching experience. He has published total 32 papers in reputed international journals. His research work focuses on compression & encryption algorithm related to text, audio & video data. His area of interest is Data communication, Network & Data security, Fuzzy logic & neural network.

