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GaN channel Nanoscale MOSFET with Silicon Source and Drain and Silicon Germanium Bulk

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***Abstract*—Extensive scaling in Conventional MOSFETs lead to degradation to their electrical parameters. This work proposes a GaN channel Nanoscale MOSFET for improvement in Electron Mobility, Off current with satisfactory On current, Threshold voltage and Subthreshold Swing Off current of the order of 10^{-11} A/um and Electron Mobility of around 1300 cm^2/ V-s are obtained.**

***Index Terms*—MOSFET, GaN, Silicon Germanium, On-Off current ratio, mobility**

INTRODUCTION

High speed device and high drain current at low supply voltage is need of present day advancement of semiconductor technology. In MOSFETs, low mobility and high off state leakage current is matter of concern in comparison to advanced device like High Electron Mobility Transistors (HEMTs). Group III-V [1] compound semiconductors are an efficient replacement as a channel material for silicon in conventional MOSFET to improve high drive current for fast switching at low off state leakage current. Various structures has been already proposed for improvement of conventional MOSFETs such as MOSFETs [2], DG MOSFETs [3], Junctionless DG MOSFETs [4], stacked high-k MOSFETs [5], Quantum-Well MOSFETs[6], Heterostructure and Silicon Double Gate Mosfet[7] and GaN MOSFET[8].

Moreover, in present day world requirement of high speed Nanoscale devices are needs, so mobility improvement must be taken care off. In this paper, we have proposed a new architecture of MOSFET, which improves off state leakage current along with mobility. Our model consists of group III-V compound semiconductor Gallium Nitride (GaN) as a replacement for silicon as channel and Silicon Germanium (SiGe) as substrate is used. In this work, we have varied gate dielectric and studied the various parameters for our architecture like electron mobility, I_{ON}/I_{OFF} ratio, threshold voltage and subthreshold swing. An accelerated mobility with excellent I_{ON}/I_{OFF} ratio is obtained.

The second section of this paper describes the structure and the third section discusses the simulation results obtained.

DEVICE ARCHITECTURE

The proposed structure of the MOSFET is shown in Fig. 1. Here, GaN is used as a channel with doping concentration $1x10^{17}$ cm^{-3} and SiGe as substrate with doping concentration $1x10^{18}$ and 20% Germanium concentration. Boron is used as dopant for channel and substrate. Source and drain is silicon region which are doped with n-type dopant Phosphorus and doping concentration $2x10^{18}$. Total length of the device is 120nm. The body thickness is 30nm with gate length fixed for our study at 60nm. Gate metal used here is Polysilicon and gate dielectric which are of 2nm thick.

RESULTS AND DISCUSSION

The Sentaurus TCAD is used to simulate proposed structure. The models used are

a) Fermi-Dirac statistics for presence of high doping.

b) E-HighFieldSaturation, Dopingdependence and phumob as Mobility models.

c) SRH (Dopingdependence) as Recombination models.

Our study has been done using three gate dielectrics which are Silicon Dioxide (k = 3.9), Alumina (k = 10) and Hafnium Oxide (k = 22) where k is the dielectric constant.

The linear plot of drain current versus gate voltage for different gate dielectrics is shown in Fig. 2 and logarithmic plot has been shown in Fig. 3. Simulation is done for V_{DS}=0.5V and gate voltage is ramped from 0 to 2 V. We observe that I_{ON}/I_{OFF} increases with increase in value of gate dielectric constant increases. Here, highest on current is obtained for HfO_2 and value is 3.026mA/µm. The capacitance is directly proportional to dielectric constant, as a result at higher value of dielectric constant (k), more channel inversion is obtained which is depicted by Eq. 1.

$$C = (k\varepsilon_0 A)/t_{ox} \quad (1)$$

Where, C is the capacitance, k is the dielectric constant, ε_0 is the permittivity of vacuum, A is the area of the gate and t_{ox} is the gate oxide thickness.

The variation of threshold voltage reduces for increase in dielectric constant as shown in Fig.4. Reason is well explained Eq. 1. Increase of dielectric constant increases capacitance, as a result we get inversion of channel at lower gate voltage. The threshold voltage reduces to 0.99V for HfO_2 as gate dielectric from 1.22V for SiO_2 as gate dielectric. The best result for our structure is for HfO_2 as gate dielectric.

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Fig. 5 shows the variation of electron mobility with dielectric constant and it is observed that, electron mobility increases as value of dielectric constant increases. Where, highest value for electron mobility is obtained for HfO_2 as $1.298x10^3$ cm^2/V-s.

Fig. 6 shows value of off current for different dielectrics, it is observed that off current increases as K increases, which is well explained as threshold voltage reduces results in increase in off current. SiO_2 as gate dielectric gives the lowest off current, value is $2.024x10^{-11}$ A/µm.

Fig. 7 shows plot of on current for different dielectrics. Highest on-current is obtained is $3.026x10^{-3}$ A/µm for HfO_2 as gate dielectric.

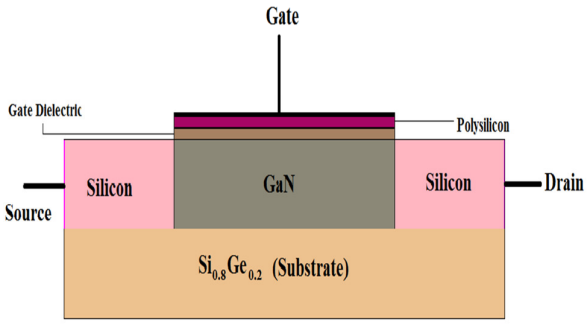
Fig. 8 shows plot of I_{on}/I_{off} ratio. An excellent value of 10^8 is achieved for k = 22. Moreover, for the other two cases too, the ratios are greater than 10^6.

Fig.9 shows plot of subthreshold swing versus variation of dielectric constant, Subthreshold Swing (SS) of a device is a measure of how well the device switches off. We observed subthreshold swing reduces with increase in gate dielectric. Whereas, SS of a MOSFET is limited to 60 mV/dec as subthreshold drain current depends on thermal voltage (kT/q). Generally, MOSFETs have SS in the range of 100 – 200 mV/dec. In this work, we have obtained low values of SS for HfO_2 as gate dielectric of the value 117.23 mV/dec.

The plot of I_D-V_{DS} for different dielectrics is shown in Fig. 10 for V_{GS} equal to 1.5 V.

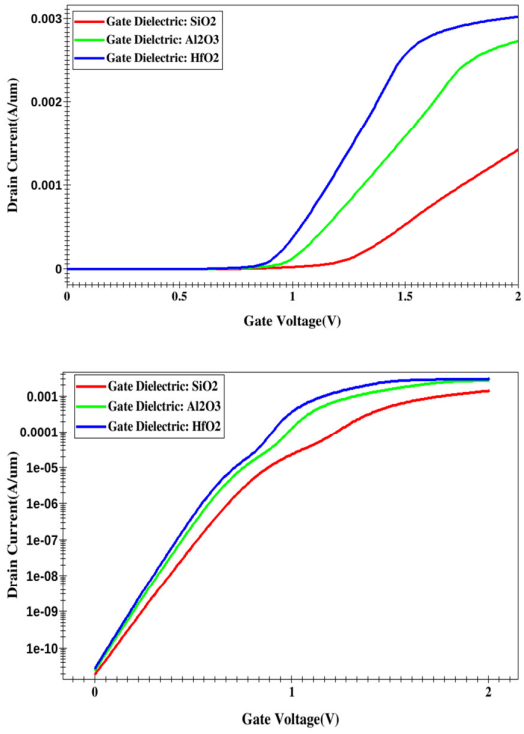
CONCLUSION

The proposed MOSFET structure in this work has very promising outcome for the semiconductor world. The I_{on}/I_{off} ratio is satisfactorily improved along with high on-current and electron mobility, which make this device useful for digital application. The best suited observed gate dielectric for proposed structure is HfO_2. The scope of this work may be extended to improving the SS without degrading the on-current and electron mobility.

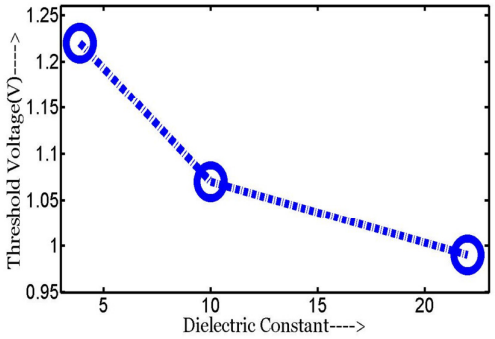


2D structure of the proposed MOSFET

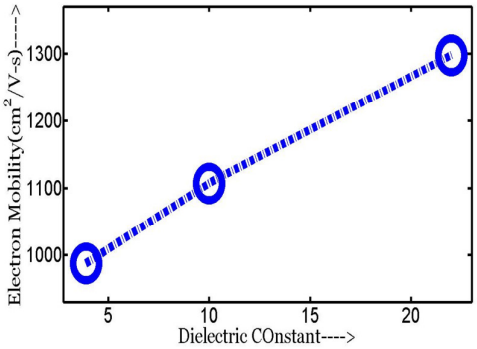
Linear plot of Drain Current versus Gate Voltage for fixed drain voltage at 0.5 V.



Logarithmic plot Drain Current versus Gate Voltage for fixed drain voltage of 0.5V.



Threshold Voltage variation with various Gate Dielectric constant (K) at drain voltage of 0.5 V



Electron Mobility variation with various Gate Dielectric Constant (K) at drain voltage of 0.5V.

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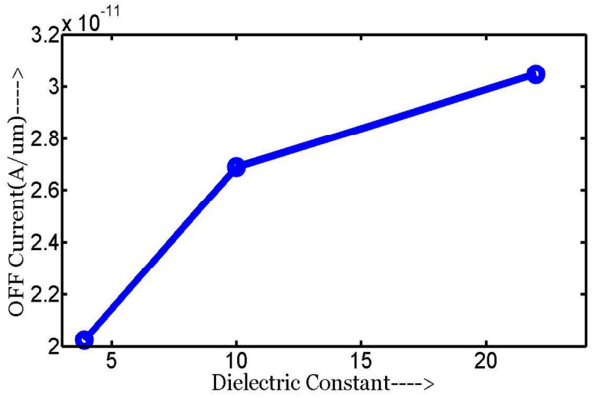
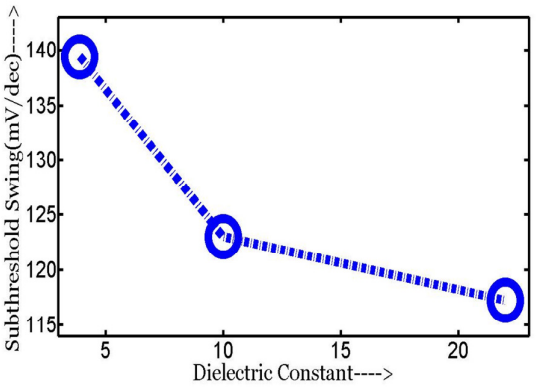
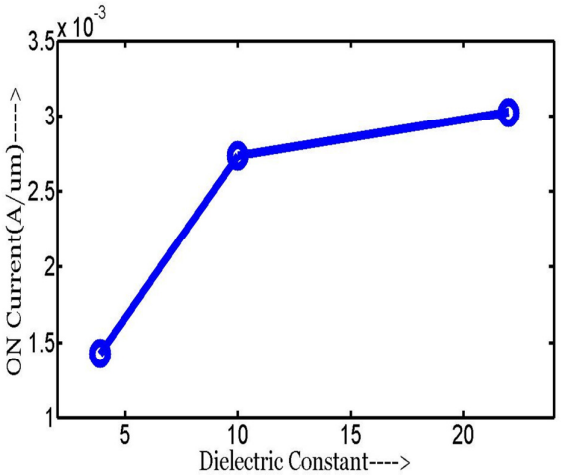


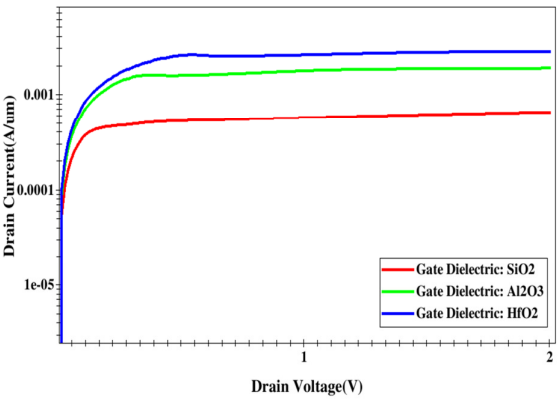
OFF current variation with various Gate Dielectric Constant(K) at drain voltage of 0.5 V



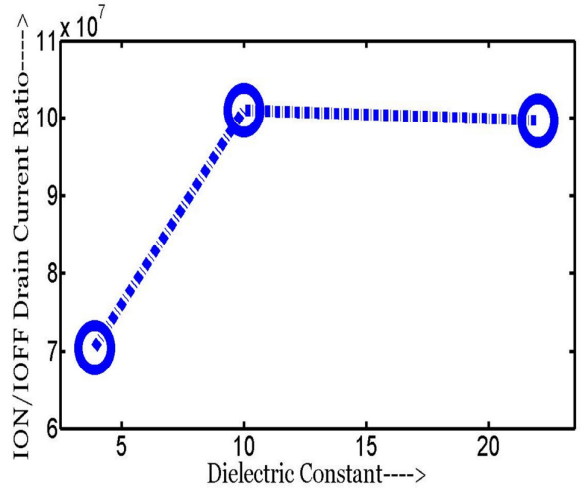
Subthreshold Swing variation with various Gate Dielectric constant(K) at drain voltage of 0.5 V



ON current variation with various Gate Dielectric constant(K) at drain voltage of 0.5 V



Drain Current versus Drain Voltage plot for different gate dielectric constants for Gate Voltage of 1.5 V



ON-OFF current ratio with various Gate Dielectric constant(K) at drain voltage of 0.5 V

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