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A Comparative Study of Full Adder Using Different Logic Style

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***Abstract*—** In recent year, power dissipation is one of the biggest challenges in VLSI design. Adder circuits are the main sources of power dissipation in signal processing units. By reducing the number of transistors in the circuits and the design structures are may occupied small area and low power design. In this paper a Full Adder Circuit is designed by using CMOS, Transmission gates and pass Transistor logic and the power and delay are analysed. Power consumption and speed are two important but conflicting design aspects; hence a better way to evaluate circuit performance is power delay product (PDP). The designs are implemented and power, delay results are obtained by using TANNER EDA Tool. The results show that the transistor counts, delay and the power required are significantly concentrated in the design.

***Keywords*—** Full Adder, CMOS, Transmission Gate (TG), Pass Transistor, Power Dissipation, Delay, PDP

I. INTRODUCTION

Adders are the key element in many VLSI systems such as microprocessors, ALU"s, multiplexers, comparators, parity checkers, digital signal processing (DSP) architectures, code converters etc. Moore's law describes the requirement of the transistors for VLSI design it gives the practical observation that number of transistor density and performance of integrated circuits (IC), doubling every two years. The design of adder circuits forms the basic building blocks of all digital VLSI design circuits has been undergoing considerable improvements, being driven by three basic design goals, viz. reducing the transistor counts i.e. reducing the area, minimizing the power consumption and increasing the speed of operation. Great effort has been determined on low-power microelectronics due to high-speed development of processors, digital equipment's, portable systems and cellular networks [1][2][3][4].

The design criterion of a full adder involves transistor counts which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU).

For performance analysis of various full adders different parameters are measured like power dissipation, delay, number of transistors used and power delay product of circuit.

Now, power dissipation depends on switching activity, the number and size of transistors, node capacitance, wiring complexity etc.

$$P_{avg} = P_{static} + P_{dynamic} + P_{short\text{-}circuit}$$

The energy consumed by gate per switching element is known as PDP which is also called "Figure-of-Merit". The power delay product is a measure of efficiency in an adder circuit. There is a trade-off between power dissipation and speed and is very important when low power operations are needed [4]. It is given by:

$$PDP = Power * DELAY$$

Reducing the number of transistors may lead to reduced power but sometime does not improve. Unit of PDP is fJ that is femto joule. Where femto joule means 10^{-15}= 1 fJ

II. LOGIC STYLES USED

A. CMOS Technology

CMOS technology is the One of the most popular MOSFET technologies available today. This technology makes use of both P and N channel devices in the same substrate material. Such devices are extremely useful, since the *same* signal which turns *on* a transistor of one type is used to turn *off* a transistor of the other type. This allows the design of logic devices using *only* simple switches, without the need for a pull-up resistor [1].

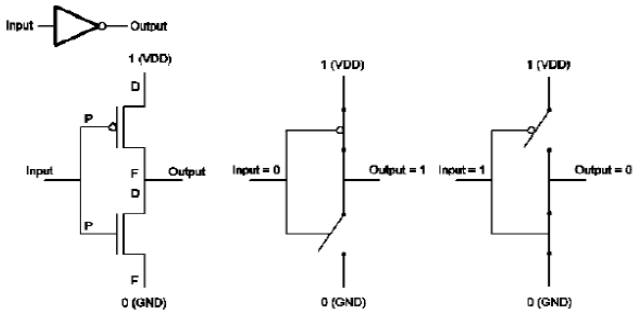

Fig 1: The basic operation of CMOS

B. Transmission Gate

A transmission gate, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a pMOS transistor and nMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node active-low A, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low A is a Logic 0, the complementary Logic 1 is applied to node A, turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes [1].

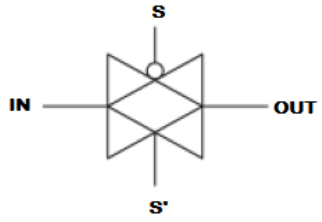

Fig 2: Circuit Symbol of TG

C. Pass Transistor Logic

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used. Pass Transistor uses only an n-MOSFET network for the implementation of logic functions, thus resulting in low input capacitance and high speed operation. The high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. The advantages of pass logic transistors include – Smaller number of transistors and smaller input loads, along with MUX and especially XOR circuits being implemented efficiently [1].

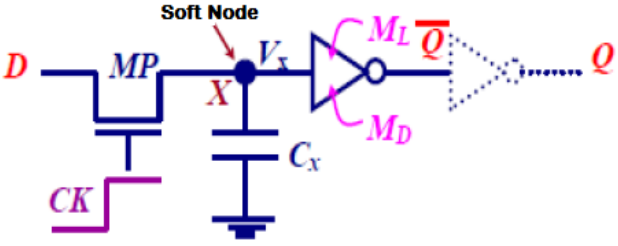

Fig 3: Circuit Symbol of Transmission Gate

III. Full Adder Design using different logic Style

The various logic styles discussed above can be used for implementing different elements of Arithmetic unit. Each of the circuit style has its own advantages and disadvantages. Full Adder is the basic design element of any Arithmetic Unit aiming to achieve three basic design goals such as minimizing the power consumption, minimizing the transistor count and increasing the speed. Minimizing the transistor count will lead to lower power consumption, as well as high speed. Description of static conventional full adder circuit given below.

Adder is a circuit that operates for a given three 1-bit inputs A, B, C and two 1-bit outputs sum and carry.

$S = A \oplus B \oplus C$ *(i)*

$S = C' . (A \oplus B) + C(A \odot B)$ *(ii)*

$Carry = A.B + C(A \oplus B) = C(A \oplus B) + A(A \odot B)$ *(iii)*

$A \oplus B = A'B + AB'$ *(iv)*

$A \odot B = A.B + A'B'$ *(v)*

Where 'S' was denoted as 'Sum'.

In this work the full adder circuits are designed with the help of 900nm of PMOS, 450nm of NMOS technology.

The design details of full adder implemented using three different logic styles viz. CMOS, Transmission Gate and Pass Transistor Logic are given below [4][5].

A. CMOS Based Full Adder

CMOS Full Adder consists of 28 transistors in each full transistor. The schematic diagram of CMOS full Adder is designed using Cadence tool shown in figure 4. The design has been simulated at 900nm of PMOS, 450nm of NMOS technology [6].

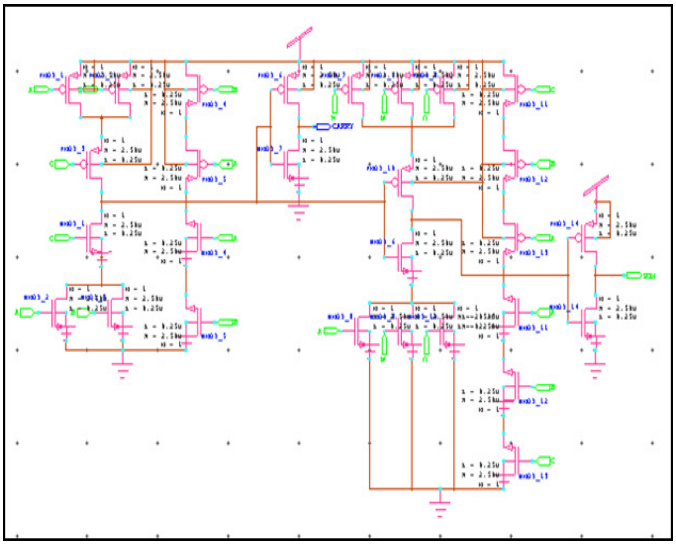

Fig 4: Schematic of CMOS based Full Adder

B. *Transmission Gate Based Full Adder*

Transmission Gate Full Adder uses 22 transistors to implement the sum and carry logic. Transmission Gate Full Adder performs better than CMOS Full Adder in case of power dissipation as well as delay with lesser number of transistors being used [4][5][6]. The overall schematic diagram of Full Adder using Transmission Gate has been described in figure 5.

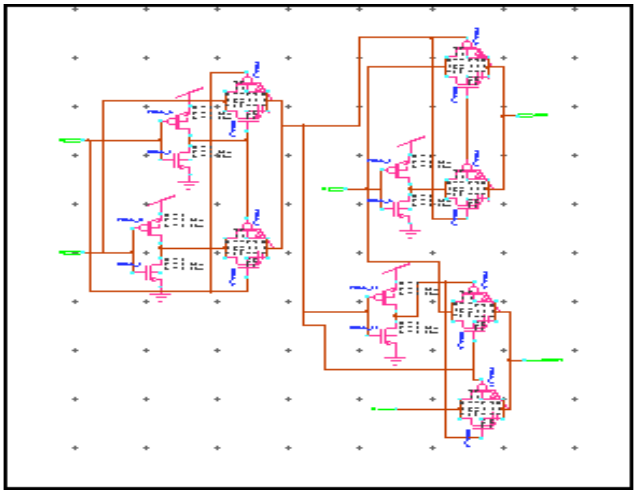

Fig 5: Schematic of TG based Full Adder

C. *Pass Transistor Based Full Adder*

The proposed 10-transistor Full Adder is designed using Pass Transistor logic. It uses lesser number of transistors than the above two. Power dissipation is quite less in this case [5][6]. The schematic diagram of fill adder using pass transistor logic has been described in figure 6.

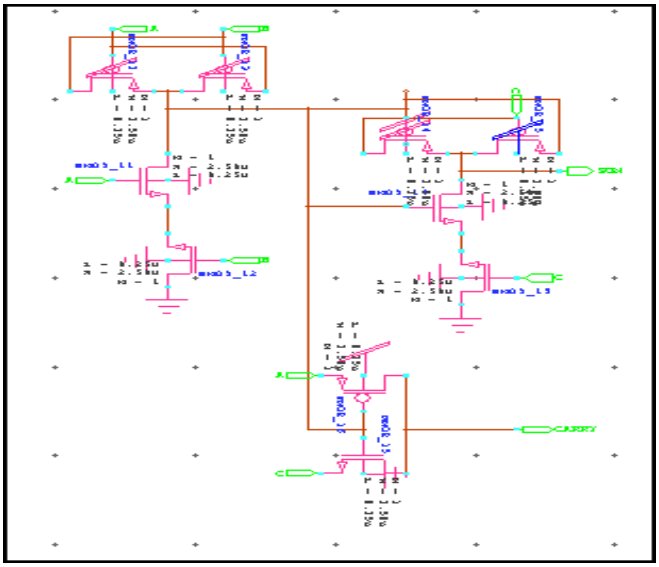

Fig 6: Schematic of Pass Transistor based Full Adder

IV. Performance Analysis & Simulation

In this paper the Full Adder Circuit is compared based on the performance parameters like propagation delay, power dissipation, number of transistors with the help of different logic styles. The channel width of the transistors is 450n for the NMOS and 900nm for the PMOS. In this work all the circuits have been designed using TANNER EDA with model file as dual.md. To achieve low power and high performance multipliers these are tested at 5v so, that the performance of multipliers can be improved. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention. For simulation method T-spice is used in order to analyze the results. The comparative results Full Adder circuit for different logic design styles are given in Table 1.

Table 1: Comparisons of performance parameters for different logic styles

Circuit Techniques	Power Dissipation(µw)	Delay(ns)	PDP(fJ)	No.of Transistor
CMOS	460	1.1	506	28
Transmission Gate	352	0.078	27.45	22
Pass Transistor	82	0.08	6.56	10

A bar graph is plotted for delay (ns) and power dissipation (µw) and No. of Transistors of Full Adder Circuit for the logic used here as shown in Fig.7, Fig.8, Fig.9, and Fig.10 respectively.

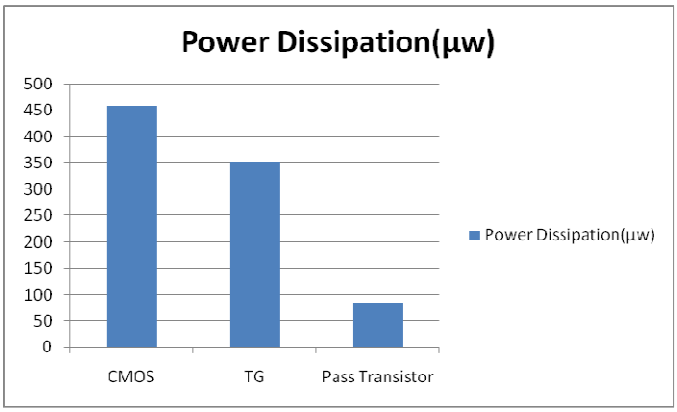

Fig 7: Power Dissipation variation

As shown in the above figure that using pass transistor model of full adder circuit dissipate less power than other logic style.

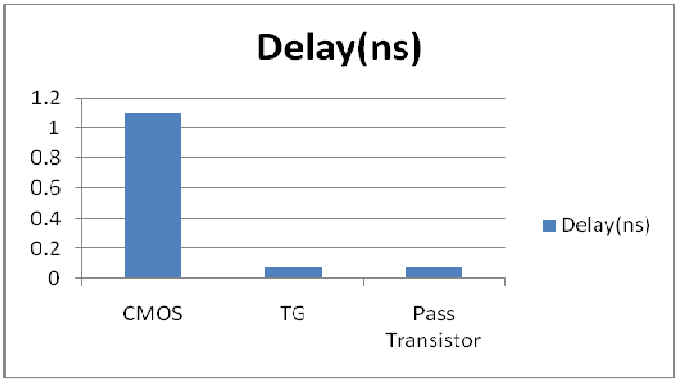

Fig 8: Delay variation

As shown in the above figure that using pass transistor model of full adder circuit has less delay than other logic style.

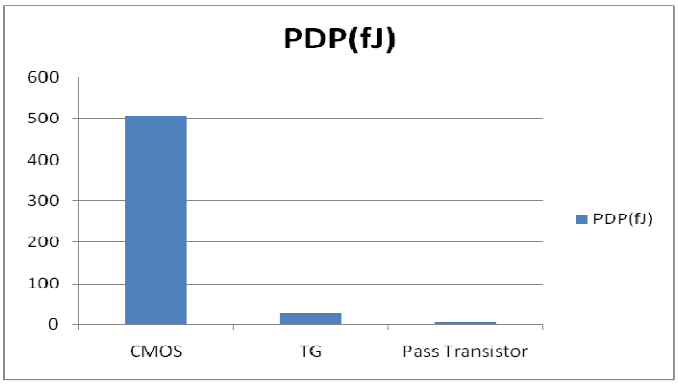

Fig 9: PDP variation

As shown in the above figure that using pass transistor model of full adder circuit has improve the PDP value than other logic style.

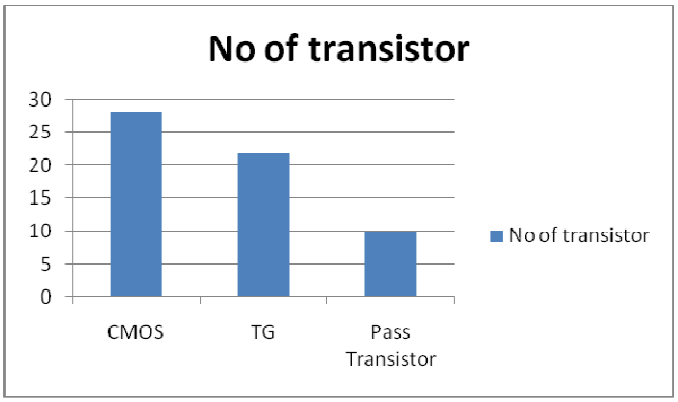

Fig 10: Performance Comparison of No. of Transistor

As shown in the above figure that using pass transistor model of full adder circuit use less number of transistors than other logic style.

V. CONCLUSION

In this paper it has been observed that pass transistor (CPL) logic design style exhibit better characteristics as compared to other design styles. So, pass transistor logic style can be used where portability and high speed is the prime aim. CMOS consumes the highest power among the three. But, the pass transistor logic design style has propagation delay is higher than transmission gate logic style, so pass transistor logic can be considered best logic design style with respect to all parameters of Full Adder Circuit Design. In this paper it will also observed that the number of transistors used is significantly reduced resulting in a great reduction in switching activity. Besides, due to its dynamic characteristic, short circuit current is eliminated. This considerable reduction in power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP as shown in the observation table.

VI. ACKNOWLEDGEMENT

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